In the Claims:

1. (Currently amended) A ferroelectric memory device comprising:

a semiconductor substrate;

a lower interlayer dielectric on the semiconductor substrate;

a plurality of ferroelectric capacitors on the lower interlayer dielectric; and

a plate line that extends across and electrically connects to surfaces of at least two adjacent ones of the plurality of ferroelectric capacitors, wherein sidewalls of the ferroelectric capacitors are substantially vertical relative to a top surface of the semiconductor substrate.

2. (Original) The device as claimed in claim 1, further comprising:

an upper interlayer dielectric on the lower interlayer dielectric and the plurality of ferroelectric capacitors; and

hydrogen barrier spacers between sidewalls of the ferroelectric capacitors and the lower interlayer dielectric.

3. (Original) The device as claimed in claim 2, wherein the hydrogen barrier spacers are at least one from the group consisting of TiO_2, Al_2O_3, ZrO_2, and CeO_2.

4. (Original) The device as claimed in claim 2, wherein the plate line covers sidewalls of the hydrogen barrier spacers and a surface of the lower interlayer dielectric.

5. (Original) The device as claimed in claim 1, wherein the plate line comprises:

a local plate line directly contacting the surfaces of the at least two adjacent ferroelectric capacitors; and

a main plate line on the upper interlayer dielectric opposite to the local plate line and directly contacting a surface of the local plate line via a slit-type via hole

through the upper interlayer dielectric.

6. (Original) The device as claimed in claim 5, wherein the upper interlayer dielectric is between the local plate line and main plate line.

7. (Original) The device as claimed in claim 1, wherein the plurality of ferroelectric capacitors are arranged in rows and columns.

8. (Canceled).

9. (Currently amended) The device as claimed in ~~claim 8~~claim 1, wherein sidewalls of the ferroelectric capacitors have an inclination of about 70° to about 90° relative to a top surface of the semiconductor substrate.

10. (Original) The device as claimed in claim 1, wherein the ferroelectric capacitor comprises a lower electrode, a ferroelectric pattern, and an upper electrode, wherein the plate line directly contacts the upper electrodes of at least two adjacent ones of the plurality of ferroelectric capacitors.

11. (Currently amended) A ferroelectric memory device comprising:

a semiconductor substrate;

a lower interlayer dielectric on the semiconductor substrate;

a plurality of ferroelectric capacitors on the lower interlayer dielectric; and

a plate line that extends across and electrically connects to surfaces of at least two adjacent ones of the plurality of ferroelectric capacitors, wherein the ferroelectric capacitor comprises a lower electrode, a ferroelectric pattern, and an upper electrode, wherein the plate line directly contacts the upper electrodes of at least two adjacent ones of the plurality of ferroelectric capacitors, and ~~The device as claimed in claim 10,~~ wherein the lower electrode and the upper electrode comprise at least one of ruthenium and ruthenium oxide.

12. (Currently amended) A ferroelectric memory device comprising:

a semiconductor substrate;

a lower interlayer dielectric on the semiconductor substrate;

a plurality of ferroelectric capacitors on the lower interlayer dielectric; and

a plate line that extends across and electrically connects to surfaces of at least two adjacent ones of the plurality of ferroelectric capacitors, wherein the ferroelectric capacitor comprises a lower electrode, a ferroelectric pattern, and an upper electrode, wherein the plate line directly contacts the upper electrodes of at least two adjacent ones of the plurality of ferroelectric capacitors, and ~~The device as claimed in claim 10,~~ wherein the ferroelectric pattern comprises PZT(Pb, Zr, TiO_3) with $PbTiO_3$ as a seed layer.

13. (Original) The device as claimed in claim 10, wherein the ferroelectric pattern is at least one material from the group consisting of $SrTiO_3$, $BaTiO_3$, (Ba, Sr)TiO_3, Pb(Zr,Ti)O_3, $SrBi_2Ta_2O_9$, (Pb,La)(Zr,Ti)O_3, and $Bi_4Ti_3O_{12}$.

14. (Original) The device as claimed in claim 1, wherein the plate line is at least one material from the group consisting of the platinum group including ruthenium, platinum, iridium, rhodium, Osmium, and palladium, and oxides thereof.

15. (Original) The device as claimed in claim 1, wherein the plate line is a local plate line directly contacting the surfaces of at least two adjacent ones of the plurality of ferroelectric capacitors, and further comprising an upper interlayer dielectric covering the local plate line.

16. (Original) The device as claimed in claim 1, further comprising an upper interlayer dielectric covering on the plurality of ferroelectric capacitors, and wherein the plate line is a main plate line directly contacting the surfaces of the at least two adjacent ones of the plurality of ferroelectric capacitors via a slit-type via

hole penetrating the upper interlayer dielectric.

17. (Original) The device as claimed in claim 1, further comprising an insulation pattern between the plate line and the lower interlayer dielectric.

18. (Original) The device as claimed in claim 17, wherein the insulation pattern is an upper interlayer dielectric.

19. (Original) The device as claimed in claim 1, further comprising an upper interlayer dielectric on the plurality of ferroelectric capacitors, and main word lines on the upper interlayer dielectric.

20. (Currently amended) A method of fabricating a ferroelectric memory device, comprising:

forming a lower interlayer dielectric on a semiconductor substrate;

forming a plurality of ferroelectric capacitors on the lower interlayer dielectric; and

forming a plate line that extends across and electrically connects to surfaces of at least two adjacent ones of the plurality of ferroelectric capacitors, wherein sidewalls of the ferroelectric capacitors are formed to be substantially vertical relative to a top surface of the semiconductor substrate.

21. (Original) The method as claimed in claim 20, further comprising:

forming hydrogen barrier spacers between sidewalls of the ferroelectric capacitors and the lower interlayer dielectric; and

forming an upper interlayer dielectric on the lower interlayer dielectric and the plurality of ferroelectric capacitors.

22. (Original) The method as claimed in claim 21, wherein the hydrogen barrier spacers are formed from a material selected from one or more of the group

consisting of TiO_2, Al_2O_3, ZrO_2, and CeO_2.

23. (Original) The method as claimed in claim 21, wherein the forming a plate line comprises forming the plate line on sidewalls of the hydrogen barrier spacers and a surface of the lower interlayer dielectric.

24. (Original) The method as claimed in claim 21, wherein forming the plate line comprises:

forming a lower plate layer on the semiconductor substrate and the hydrogen barrier spacers; and

pattering the lower plate layer to form a plurality of parallel local plate lines,

wherein each of the local plate lines directly contacts surfaces of at least two adjacent ones of the plurality of ferroelectric capacitors.

25. (Original) The method as claimed in claim 24, wherein prior to the forming the lower plate line, the method further comprises:

forming an insulation layer on the semiconductor substrate and the hydrogen barrier spacers; and

planarizing the insulation layer until surfaces of the ferroelectric capacitors are exposed, and leaving an insulation pattern filling a gap region between the ferroelectric capacitors.

26. (Original) The method as claimed in claim 24, wherein after forming the local plate line, the method further comprises sequentially forming a first upper interlayer dielectric layer and a second upper interlayer dielectric layer on the local plate lines.

27. (Original) The method as claimed in claim 26, further comprising:

successively patterning the second and first interlayer dielectric layers to form a slit-type via hole exposing a portion of the local plate lines; and

forming a main plate line covering the slit-type via hole.

28. (Original) The method as claimed in claim 20, wherein forming a plurality of ferroelectric capacitors comprises:

sequentially forming a lower electrode layer, a ferroelectric layer, and an upper electrode layer on the lower interlayer dielectric; and

successively patterning the upper electrode layer, the ferroelectric layer, and the lower electrode layer to form a plurality of stacked lower electrode, ferroelectric pattern, and upper electrode structures that are arranged in row and column directions.

29. (Currently amended) The method as claimed in ~~claim 28~~claim 20, wherein sidewalls of the ferroelectric capacitors have an inclination of about 70° to about 90° relative to a top surface of the semiconductor substrate.

30. (Currently amended) A method of fabricating a ferroelectric memory device, comprising:

forming a lower interlayer dielectric on a semiconductor substrate;

forming a plurality of ferroelectric capacitors on the lower interlayer dielectric; and

forming a plate line that extends across and electrically connects to surfaces of at least two adjacent ones of the plurality of ferroelectric capacitors, wherein forming a plurality of ferroelectric capacitors comprises:

sequentially forming a lower electrode layer, a ferroelectric layer, and an upper electrode layer on the lower interlayer dielectric; and

successively patterning the upper electrode layer, the ferroelectric layer, and the lower electrode layer to form a plurality of stacked lower electrode, ferroelectric pattern, and upper electrode structures that are arranged in row and column directions, and ~~The method as claimed in claim 28,~~ wherein the lower electrode layer and the upper electrode layer are formed from at least one of ruthenium and ruthenium oxides.

31. (Currently amended) A method of fabricating a ferroelectric memory device, comprising:

forming a lower interlayer dielectric on a semiconductor substrate;

forming a plurality of ferroelectric capacitors on the lower interlayer dielectric; and

forming a plate line that extends across and electrically connects to surfaces of at least two adjacent ones of the plurality of ferroelectric capacitors, wherein forming a plurality of ferroelectric capacitors comprises:

sequentially forming a lower electrode layer, a ferroelectric layer, and an upper electrode layer on the lower interlayer dielectric; and

successively patterning the upper electrode layer, the ferroelectric layer, and the lower electrode layer to form a plurality of stacked lower electrode, ferroelectric pattern, and upper electrode structures that are arranged in row and column directions, and ~~The method as claimed in claim 28,~~ wherein successively patterning the upper electrode layer, the ferroelectric capacitor layer, and the lower electrode layer comprises anisotropically etching using a plasma containing oxygen.

32. (Currently amended) A method of fabricating a ferroelectric memory device, comprising:

forming a lower interlayer dielectric on a semiconductor substrate;

forming a plurality of ferroelectric capacitors on the lower interlayer dielectric; and

forming a plate line that extends across and electrically connects to surfaces of at least two adjacent ones of the plurality of ferroelectric capacitors, wherein forming a plurality of ferroelectric capacitors comprises:

sequentially forming a lower electrode layer, a ferroelectric layer, and an upper electrode layer on the lower interlayer dielectric; and

successively patterning the upper electrode layer, the ferroelectric layer, and the lower electrode layer to form a plurality of stacked lower electrode, ferroelectric pattern, and upper electrode structures that are arranged in row and column directions,

and ~~The method as claimed in claim 28,~~ wherein the ferroelectric pattern is formed from at least one material in the group consisting of PZT(Pb, Zr, TiO_3), $SrTiO_3$, $BaTiO_3$, (Ba, Sr)TiO_3, Pb(Zr,Ti)O_3, $SrBi_2Ta_2O_9$, (Pb,La)(Zr,Ti)O_3, and $Bi_4Ti_3O_{12}$, and wherein the ferroelectric pattern is formed using $PbTiO_3$ as a seed layer.

33. (Currently amended) A method of fabricating a ferroelectric memory device, comprising:

forming a lower interlayer dielectric on a semiconductor substrate;

forming a plurality of ferroelectric capacitors on the lower interlayer dielectric; and

forming a plate line that extends across and electrically connects to surfaces of at least two adjacent ones of the plurality of ferroelectric capacitors, wherein forming a plurality of ferroelectric capacitors comprises:

sequentially forming a lower electrode layer, a ferroelectric layer, and an upper electrode layer on the lower interlayer dielectric; and

successively patterning the upper electrode layer, the ferroelectric layer, and the lower electrode layer to form a plurality of stacked lower electrode, ferroelectric pattern, and upper electrode structures that are arranged in row and column directions, and ~~The method as claimed in claim 28,~~ wherein the ferroelectric layer is formed using a chemical solution deposition using a precursor of at least one of lead acetate[$Pb(CH3CO_2)_2$ $3H_2O$], zirconium n-butoxide [$Zr(n\text{-}OC_4H_9)_4$], and titanium isopropoxide [$Ti(i\text{-}OC_3H_7)_4$], and using a solvent 2-methoxyethano [$CH_3OCH_2CH_2OH$].

34. (Original) The method as claimed in claim 21, wherein the forming the hydrogen barrier spacers comprises:

conformally forming a hydrogen barrier layer on the ferroelectric capacitors and the semiconductor substrate; and

anisotropically etching the hydrogen barrier layer until surfaces of the ferroelectric capacitors are exposed,

wherein the hydrogen barrier layer is formed from at least one material selected from the group consisting of TiO_2, Al_2O_3, ZrO_2, and CeO_2.

35. (Original) The method as claimed in claim 21, wherein forming the upper interlayer dielectric and the forming the plate line comprises:

sequentially forming first and second upper interlayer dielectrics on the hydrogen barrier spacers and the semiconductor substrate; and

successively patterning the second and first upper interlayer dielectrics to form a slit-type via hole exposing a surface of the ferroelectric capacitor in a row direction; and

forming a main plate line covering the slit-type via hole.

36. (Original) The method as claimed in claim 35, wherein the slit-type via hole exposes a surface of the lower interlayer dielectric between the ferroelectric capacitors.

37. (Original) The method as claimed in claim 35, wherein the forming the slit-type via hole comprises leaving a portion of the first upper interlayer dielectric between the hydrogen barrier spacers.

38. (Original) The method as claimed in claim 35, wherein the sequentially forming first and second upper interlayer dielectrics comprises forming main word lines between the first and second upper interlayer dielectrics.